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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,848	06/19/2003	Jonathan B. Ballagh	X-1192 US	7556
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XILINX, INC ATTN: LEGAL DEPARTMENT 2100 LOGIC DR SAN JOSE, CA 95124			EXAMINER PIERRE LOUIS, ANDRE	
			ART UNIT 2123	PAPER NUMBER
			MAIL DATE 09/17/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/600,848

Applicant(s)

BALLAGH ET AL.

Examiner

Andre Pierre-Louis

Art Unit

2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 August 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters; prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 08/07/2007 has been entered.

2. Claims 1-27 are presented for examination.

Response to Arguments

3. Applicant's arguments filed 06/26/2007 have been fully considered but they are not persuasive.

3.1 Applicants again argue that the reference relied upon does not achieve clock stabilization as claimed, the Examiner respectfully disagrees and notes that the combined teachings of the cited references are clearly mapped to show what is relied upon to teach the clock stabilization of the instant claim and evidence can be found in the ground of rejection below along with the response to arguments previously submitted. However, the Examiner further asserts that Yamaoka et al. (*see col.23 lines 1-9 and fig.28 (163), col.20 lines 11-22*) does provide the teaching for the clock stabilization of the instant claims and is clearly mapped and fully support the rejection of the claims, as shown below. Although a small portion of the cited references was used in the rejection, the Examiner notes that the references should be considered entirely by the Applicants. The Examiner further notes that the rejection relied on the combined reference used in the rejection and further encouraged the Applicants to review the references cited not used shown below and in the previous action.

3.2 Regarding Appellant's notes of establishing a *prima facie* case of obviousness is acknowledged. However, the Examiner notes that the ground of rejection below clearly shows a complete mapping of the cited prior art to the instant claims addressing all claims limitations, the cited reference used are clearly analogous art because they are from the same of endeavor. The Examiner, in the above ground of rejection, points to specific portion of the references for reasons/motivation to combine the references and therefore the Examiner has properly rejection the claims in accordance with the practices and procedures set forth in the MPEP.

3.3 While the Applicant believes that the independent claims along with their dependencies should be found allowable, the Examiner respectfully disagrees and asserts that the combined teachings the cited references teach the entire claimed invention, as evidenced by the grounds of rejection below along the response to arguments. Found the Applicant's arguments non-persuasive, the Examiner maintains the rejection of the independent claims along with their dependencies.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out

the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4.0 Claims 1-27 rejected under 35 U.S.C. 103(a) as being unpatentable over Hassoum (U.S. Patent No. 6, 487,648), in view of Read et al. (U.S. Patent No. 5,625,580), and further in view of Yamaoka et al. (U.S. Patent No. 5,920,6000).

4.1 In considering the independent claims 1 and 14, and, Hassoum substantially teaches an apparatus for clock stabilization detection for hardware simulation, in particular a digital clock module (*fig.3 (300)*) for receiving an input clock signal and a feedback clock signal and for providing an output clock signal, the digital clock module configured to lock the feedback clock signal relative to the input clock signal and configured to produce a least common multiple (LCM) clock signal and a lock signal (*see col.2 line 14-65*); a state machine (*fig.3 (302)*) for receiving the lock signal and the LCM clock signal and configured to provide a control signal at least partially responsive to the LCM clock signal and the lock signal (*see col.2 lines 14-65*); and a select circuit (*fig.3 (306)*) for receiving the control signal and the output clock signal and configured to mask application of the output clock signal responsive to the control signal, wherein application of the output clock signal is masked until the output clock signal is sufficiently stabilized as indicated by the control signal for the hardware simulation (*also see col.9 line 24-col.10 line 13*). Hassoum also teaches feedback signal (*fig.3 (CLK_SDp, col.2 lines 50-61)*), control signal (*col.8 line 50-col.9 line 32*). However, Hassoum does not clearly teach that clock module is configured to produce a LCM signal. Read et al. substantially teaches a least common signal (*col.65 line 47-col.66 line 65*), and further teaches generating control and

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feedback signals (*col.52 lines 17-36, col.60 lines 65-67*) and hardware simulation (*see title*).

Hassoun, as modified by Read et al., teaches a plurality of clock detectors and a phase lock loop (PLL of Hassoun fig.5) for receiving the feedback signal CLK_FB; however, they do not clearly teach the term detecting clock stabilization, as claimed, and masking of the output. Yamaoka et al. substantially teaches detecting a stable clock signal (*col.23 lines 1-9 and fig.28 (163), col.20 lines 11-22*) and a lock signal (*col.25 lines 21-65 & col.27 lines 39-47*) and substantially teaching masking application of an output signal (*see col.11 lines 58-63*). Hassoun, Read et al., and analogous art because they are from the same of endeavor and that the phase clock circuitry teaches by Yamaoka et al. is similar to that of system and method of Read et al. in the device implementation of Hassoun. Therefore it would have been obvious to one ordinary skilled in the art at the time of the applicant's invention to combine the clock detecting system of Yamaoka et al. and the system and method of Read et al. with the device implementation of Hassoun because Read et al teaches a reliability and lower cost manufacturing system (*col.9 lines 3-5*) and further teaches an improvement modeling system (*see abstract*); and Yamaoka et al. teaches the advantage of achieving high performance easily and at low cost (*col.10 lines 22-25*).

4.2 As per claim 2, the combined teachings of Hassoun, Read et al., and Yamaoka et al. substantially teach the buffer coupled to receive the output clock signal and to provide the feedback clock signal, the output clock signal generated responsive to the input clock signal (*see Hassoun fig.4 (BUFG1), also fig.10 (1005,1006)*).

4.3 With regards to claim 3, the combined teachings of Hassoun, Read et al., and Yamaoka et al. substantially teach that the feedback clock signal is the LCM clock signal (*see Hassoun fig.3 (CLK_FBp, col.2 line 50-65)*).

4.4 Regarding claim 4, the combined teachings of Hassoum, Read et al., and Yamaoka et al. substantially teach that the digital clock module is disposed in a programmable logic device (PLD), and wherein the PLD comprises a configuration logic block configured with the state machine (*see Hassoum fig.3 (300)*).

4.5 As per claim 5 and 22, the combined teachings of Hassoum, Read et al., and Yamaoka et al. substantially teach that the state machine is a register (*see Hassoum col.11 line 1-col.12 line 57*).

4.6 With regards to claim 6, the combined teachings of Hassoum, Read et al., and Yamaoka et al. substantially teach that the control signal is configured to cause the select circuit to pass the output clock signal for at least approximate edge coincidence with another output clock signal (*see Hassoum fig.3, col.7 line 49-col.9 line 32*).

4.7 Regarding claim 7 and 9, the combined teachings of Hassoum, Read et al., and Yamaoka et al. substantially teach that the state machine comprises an edge detector configured to detect at least proximal phase alignment between the LCM clock signal and the output clock signal to provide the control signal (*see Hassoum fig.3, also col.9 lines 50-59*).

4.8 With regards to claims 8 and 13, the combined teachings of Hassoum, Read et al., and Yamaoka et al. substantially teach the method for clock stabilization detection for hardware simulation, in particular the step of: receiving an input clock signal (*see Hassoum fig.3 (CLK_P), col.10 line 14-col.11 line 45, also col.2 lines 50-65*); producing a feedback clock signal from the input clock signal (*see Hassoum fig.3 (CLK_FBp), fig.5 (CLK_FB), col.10 line 14-col.11 line 45, also col.2 lines 50-65*); producing an output clock signal from the input clock signal (*see Hassoum fig.3 (O_CLK), col.10 line 14-col.11 line 3, also col.2 lines 50-65*); locking the

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feedback clock signal relative to the input clock signal to produce a lock signal (*see Hassoun fig.5 (CLK_FB), col.9 line 58-co.10 line 13*), also *see Yamaoka et al. col.11 lines 58-63*);

generate a least common multiple clock signal (*see Read et al. col.65 line 47-col.66 line 65*);

generate a control signal at least partially responsive to the LCM clock signal and a the lock

signal (*see Hassoun et al. col.8 line 50-col.9 line 32*); masking the application of the output clock

signal responsive to the control signal, wherein application of the output is masked until the

output clock signal is sufficiently stabilized as indicated by the control signal for the hardware

simulation (*see Yamaoka et al. co.11 line 58-63*). However, Hassoun does not clearly teach that

clock module is configured to produce a LCM signal. Read et al. substantially teaches a least

common signal (*col.65 line 47-col.66 line 65*), and further teaches generating control and

feedback signals (*col.52 lines 17-36, col.60 lines 65-67*) and hardware simulation (*see title*).

Hassoun, as modified by Read et al., teaches a plurality of clock detectors and a phase lock loop

(PLL of Hassoun fig.5) for receiving the feedback signal CLK_FB; however, they do not clearly

teaches the term detecting clock stabilization, as claimed, and masking of the output. Yamaoka et

al. substantially teaches detecting a stable clock signal (*col.23 lines 1-9 and fig.28 (163), col.20*

lines 11-22) and a lock signal (*col.25 lines 21-65 & col.27 lines 39-47*) and substantially

teaching masking application of an output signal (*see col.11 lines 58-63*). Hassoun, Read et al.,

and analogous art because they are from the same of endeavor and that the phase clock circuitry

teaches by Yamaoka et al. is similar to that of system and method of Read et al. an the device

implementation of Hassoun. Therefore it would have been obvious to one ordinary skilled in the

art at the time of the applicant's invention to combine the clock detecting system of Yamaoka et

al. and the system and method of Read et al. with the device implementation of Hassoun because

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Read et al teaches a reliability and lower cost manufacturing system (*col.9 lines 3-5*) and further teaches an improvement modeling system (*see abstract*); and Yamaoka et al. teaches the advantage of achieving high performance easily and at low cost (*col.10 lines 22-25*).

4.9 As per claim 10, the combined teachings of Hassoun, Read et al., and Yamaoka et al. substantially teach the masking further masks application of the LCM clock signal responsive to the control signal (*see Yamaoka et al. col.1 (3), col.11 lines 58-63*).

4.10 With regards to claims 11 and 12, the combined teachings of Hassoun, Read et al., and Yamaoka et al. substantially teach the method for clock stabilization detection for hardware simulation, in particular the steps of obtaining a lock signal (*Yamaoka et al. (fig.32 (3016), col.25 lines 21-65), also see Hassoun fig.5*); obtaining a least common multiple clock signal provided responsive to an input clock signal, the input clock signal for providing an output clock signal (*see Read et al. col.65 line 47-col.66 line 65*), *also see Hassoun fig.4 &10*); generating a control signal at least partially responsive to the LCM clock signal and the lock signal, the control signal for masking application of an output clock signal responsive to the control signal, wherein application of the output clock signal is masked until the output signal is sufficiently stabilized as indicated by the control signal for the hardware simulation (*see Hassoun col.9 line 24-col.10 line 13*). Hassoun further teaches control signal (*col.8 line 50-col.9 line 32*) and substantially the means for detecting the phase alignment of the clock signal to generate the control signal (*fig.5 (512), col.9 lines 50-57*). However, Hassoun does not clearly teach that clock module is configured to produce a LCM signal. Read et al. substantially teaches a least common signal (*col.65 line 47-col.66 line 65*), and further teaches generating control and feedback signals (*col.52 lines 17-36, col.60 lines 65-67*) and hardware simulation (*see title*).

Hassoun, as modified by Read et al., teaches a plurality of clock detectors and a phase lock loop (PLL of Hassoun fig.5) for receiving the feedback signal CLK_FB; however, they do not clearly teaches the term detecting clock stabilization, as claimed, and masking of the output. Yamaoka et al. substantially teaches detecting a stable clock signal (*col.23 lines 1-9 and fig.28 (163), col.20 lines 11-22*) and a lock signal (*col.25 lines 21-65 & col.27 lines 39-47*) and substantially teaching masking application of an output signal (*see col.11 lines 58-63*). Hassoun, Read et al., and analogous art because they are from the same of endeavor and that the phase clock circuitry teaches by Yamaoka et al. is similar to that of system and method of Read et al. an the device implementation of Hassoun. Therefore it would have been obvious to one ordinary skilled in the art at the time of the applicant's invention to combine the clock detecting system of Yamaoka et al. and the system and method of Read et al. with the device implementation of Hassoun because Read et al teaches a reliability and lower cost manufacturing system (*col.9 lines 3-5*) and further teaches an improvement modeling system (*see abstract*); and Yamaoka et al. teaches the advantage of achieving high performance easily and at low cost (*col.10 lines 22-25*).

4.11 With regards to claim 15, the combined teachings of Hassoun, Read et al., and Yamaoka et al. substantially teach that the lock is a frequency lock, and wherein the at least proximal phase alignment is to a rising edge for all of the plurality of clock signals (*see Hassoun col.7 lines 19-46 & Yamaoka et al. col.27 line 1-col.28 line 61*).

4.12 As per claim 16, the combined teachings of Hassoun and read et al. that the select circuits are multiplexers (*see Hassoun fig.3, 10 (1001,1002); also see Yamaoka et al. fig.1&14 (3) and fig.2 (A)*).

4.13 Regarding claim 17, the combined teachings of Hassoum, Read et al., and Yamaoka et al. substantially teach that each of the multiplexers have one input terminal coupled to receive the respective one of the plurality of output clock signals and another input terminal coupled to electrical ground (*see Hassoum fig.3, 10 (1001,1002); also see Yamaoka et al. fig.1&14.(3) and fig.2 (A)*).

4.14 Regarding claim 18, the combined teachings of Hassoum, Read et al., and Yamaoka et al. substantially teach that the digital clock module is part of a field programmable gate array (FPGA) integrated circuit (*see Hassoum fig. 3(300), col.3 line 40-col.4 line 48 & col.9 line 50-col.10 line 59*).

4.15 With regards to claim 19, the combined teachings of Hassoum, Read et al., and Yamaoka et al. substantially teach that the state machine is configured in the FPGA integrated circuit with configurable logic (*see Hassoum fig. 3(302), col.3 line 40-col.4 line 48*).

4.16 As per claim 20, the combined teachings of Hassoum, Read et al., and Yamaoka et al. substantially teach that the LCM clock signal and feedback clock signal are sent to respective buffers prior to being input to the state machine and the digital clock module, respectively (*see Hassoum fig. 3,4,10, also col.9 line 58-col.11 line 45*).

4.17 With regards to claim 21, the combined teachings of Hassoum, Read et al., and Yamaoka et al. substantially teach that the buffers are multiplexers configured for buffering (*see Hassoum fig.3-5, 10, col.1 line 13-col.3 line 7*).

4.18 Regarding claim 23, the combined teachings of Hassoum, Read et al., and Yamaoka et al. substantially teach that the state machine is configured to produce another control signal for adjusting phase, the other control signal provided to the digital clock module for phase

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adjustment of at least one of the plurality of output clock signals (*see Hassoun fig.3, 5,col.7 line 49-col.9 line 32*).

4.19 As per claims 24 and 27, the combined teachings of Hassoun, Read et al., and Yamaoka et al. substantially teach the test system for clock stabilization detection for hardware simulation of an integrated circuit, in particular a computer having a processor, an input/output interface and memory, the memory for storing target test results and a test program, the input/output interface for communicating with integrated circuit (*see Read et al. fig.2 & 8*); a clock source for providing an input clock signal to the integrated circuit (*see Hassoun fig.3 (300)*); the integrated circuit configured with a clock stabilization circuit, the clock stabilization circuit configured to: produce a feedback clock signal from the input clock signal (*see Hassoun fig.3 (CLK_FBp), fig.5 (CLK_FB), col.10 line 14-col.11 line 45, also col.2 lines 50-65*); produce an output clock signal from the input clock signal (*see Hassoun fig.3 (O_CLK), col.10 line 14-col.11 line 3, also col.2 lines 50-65*); lock the feedback clock signal relative to the input clock signal to produce a lock signal (*see Hassoun fig.5 (CLK_FB), col.9 line 58-col.10 line 13*), *also see Yamaoka et al. col.11 lines 58-63*); generate a least common multiple clock signal (*see Read et al. col.65 line 47-col.66 line 65*); generate a control signal partially responsive to the LCM clock signal and a the lock signal (*see Hassoun et al. col.8 line 50-col.9 line 32*); detect at least proximal phase alignment between the LCM clock signal and the output clock signal for generation of the control signal (*fig.5 (512), col.7 line 49-col.9 line 32*); selectively apply the output clock signal to a design portion of the integrated circuit responsive to control signal, the control signal selecting application of the output after the lock signal and the output clock signal, wherein application of the output is masked until the output clock signal is sufficiently stabilized

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as indicated by the control signal for the hardware simulation (*see Hassoun col.12 lines 1-26 & co.14 lines 21-67*), *also see Yamaoka et al. co.11 line 58-63 & col.21 line 21-col.26 line 24*); the test program configured to cause test vectors to be applied responsive to the control signal, the test vectors applied to the design portion to obtain test results from the integrated circuit (*see Yamaoka et al. col.17 line 1-col.20 line 6*). However, Hassoun does not clearly teach that clock module is configured to produce a LCM signal. Read et al. substantially teaches a least common signal (*col.65 line 47-col.66 line 65*), and further teaches generating control and feedback signals (*col.52 lines 17-36, col.60 lines 65-67*) and hardware simulation (*see title*). Hassoun, as modified by Read et al., teaches a plurality of clock detectors and a phase lock loop (PLL of Hassoun fig.5) for receiving the feedback signal CLK_FB; however, they do not clearly teaches the term detecting clock stabilization, as claimed, and masking of the output. Yamaoka et al. substantially teaches detecting a stable clock signal (*col.23 lines 1-9 and fig.28 (163), col.20 lines 11-22*) and a lock signal (*col.25 lines 21-65 & col.27 lines 39-47*) and substantially teaching masking application of an output signal (*see col.11 lines 58-63*). Hassoun, Read et al., and analogous art because they are from the same of endeavor and that the phase clock circuitry teaches by Yamaoka et al. is similar to that of system and method of Read et al. an the device implementation of Hassoun. Therefore it would have been obvious to one ordinary skilled in the art at the time of the applicant's invention to combine the clock detecting system of Yamaoka et al. and the system and method of Read et al. with the device implementation of Hassoun because Read et al teaches a reliability and lower cost manufacturing system (*col.9 lines 3-5*) and further teaches an improvement modeling system (*see abstract*); and Yamaoka et al. teaches the advantage of achieving high performance easily and at low cost (*col.10 lines 22-25*).

4.20 With regards to claim 25, the combined teachings of Hassoun and read et al. that selective application of the output clock signal is done for at least approximate edge coincidence with another output clock signal (*see Hassoun col.12 lines 1-26 & co.14 lines 21-67*), also see *Yamaoka et al. co.11 line 58-63 & col.21 line 21-col.26 line 24*).

4.21 As per claim 26, the combined teachings of Hassoun and read et al. that selective application of the output clock signal is done for staggered edges with respect to another output clock signal *see Hassoun col.12 lines 1-26 & co.14 lines 21-67*), also see *Yamaoka et al. co.11 line 58-63 & col.21 line 21-col.26 line 24*)

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

5.1 Meguro (UPG_PUB No. 2004/0000939) teaches a clock generation and clock conversion circuit.

5.2 Miranda et al. (U.S. Patent No. 6,782,486) teaches an apparatus for stopping and starting a clock in a clock forwarding I/O system depending on the presence of valid data in a receive buffer.

6. Claims 1-27 are rejected and **THIS ACTION IS Non-FINAL**. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andre Pierre-Louis whose telephone number is 571-272-8636. The examiner can normally be reached on Mon-Fri, 8:00AM-4:30PM.

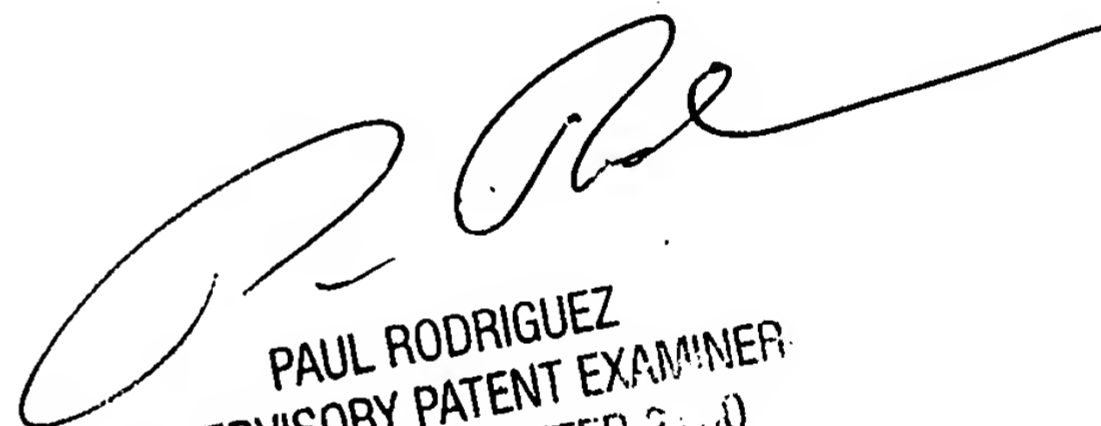
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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul L. Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

August 10, 2007

APL



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